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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/981,484	CALLWAY, EDWARD G.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,18-22 and 29-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,18,19,21,22 and 29-39* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 29-39 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments, see pages 7-8, filed May 8, 2007, with respect to the rejection(s) of claim(s) 30, 31, 38, and 39 under 35 U.S.C. 102(b) and claims 29 and 32-37 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Walls (US006215486B1) in view of Lengyel (US006016150A).

3. Applicant argues that Taylor (US006118461A) does not teach that the graphics devices each render an entire frame of video (pages 7-8).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Walls in view of Lengyel.

4. Applicant's arguments filed May 8, 2007 with respect to Claims 1, 18, 19, 21, and 22 have been fully considered but they are not persuasive.

5. With regard to Claims 1, 18, and 29, Applicant argues that the modules taught by Normile (US005461679A) are video compression and decompression modules, and do not teach

graphic devices, which perform at least graphic calculations (e.g., lighting operations, etc.) (page 8).

In reply, the Examiner points out that Taylor, which is the main reference, teaches graphic devices (Col. 4, lines 46-57). Normile is merely used for its teaching of how the video output ports are coupled.

Applicant argues that Normile does not teach a second video output port coupled to the first video component output of the second graphics device. Normile does not teach a first video component output of the second graphics device coupled to both a first video output port and a second video output port (page 9). Data from compression/decompression modules 401-404 is not deposited via the first video component output. Instead, frame buffer 430 can only receive data from bus 420, i.e., a second video output component (page 10).

In reply, the Examiner points out that bus 420 of Normile is considered to be the first video component output of the second video device (402), not frame buffer 430. Frame buffer 430 is considered to be the second video output port, not the first video component output of the second video device (402). Bus 420 is coupled to both a first video output port (425) (*shared memory 405 is coupled to bus 425 and is further coupled to bus 420*, Col. 9, lines 48-50) and a second video output port (430) (*frame buffer 430 is directly coupled to the video bus 420*, Col. 10, lines 7-11). The second video output port (430) is coupled to the first video component output (420) of the second video device (402) (*frame buffer 430 is directly coupled to the video bus 420, the structure of module 401 has equal application to each of the remaining compute modules such as 402-404, grant compute module 401 access to shared memory 405 over bus 420,* Col. 10, lines 7-11, 25-27, 55-57; *multiple video processing modules such as 401-404*, Col.

9, lines 11-15). Therefore, Normile teaches a first video device (401; *multiple video processing modules such as 401-404*, Col. 9, lines 11-15) having a first video component output (412) (*modules 401-404 are coupled to a computer system bus 425 via control bus 412,* Col. 9, lines 15-17); a second video device (402) having a first video component output (420) (*the structure of module 401 has equal application to each of the remaining compute modules such as 402-404, grant compute module 401 access to shared memory 405 over bus 420,* Col. 10, lines 25-27, 55-57); a first video output port (425) coupled to the first video component output (412) of the first video device (401) (*modules 401-404 are coupled to a computer system bus 425 via control bus 412,* Col. 9, lines 15-17) and the first video component output (420) of the second video device (402) (*shared memory 405 is coupled to bus 425 and is further coupled to bus 420*, Col. 9, lines 48-50; Col. 10, lines 25-27, 55-57); and a second video output port (430) coupled to the first video component output (420) of the second video device (402) (*frame buffer 430 is directly coupled to the video bus 420,* Col. 10, lines 7-11, 25-27, 55-57), as recited in Claim 1.

6. With regard to Claims 19, 21, and 22, Applicant argues that Taylor does not teach any component that is capable of determining a value of the first signal at a first output node. Instead, the digital to analog converter does exactly what the Examiner cited: "receives digital data from controller 104 and outputs the analog data to drive display 110 in response" (pages 10-11).

In reply, the Examiner points out that since the digital to analog converter receives digital data (first signal) from controller 104 (first output node) and outputs analog data to drive the display in response to the first signal from the first output node, it must inherently determine a

value of the first signal in order to output analog data, since it outputs analog data in response to the first signal. This means that the determined value of the first signal causes the digital to analog converter to output analog data.

Applicant argues that Deering (US005963200A) does not teach adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node. Deering describes that a master emits the FIELD signal, thereby causing the slaves to reset the counters (horizontal and vertical dimensions) which produce the video timing signals such as horizontal synch, vertical synch, and blanking. Thus, for example, the vertical blanking occurs nearly simultaneously on different video displays 25. Also, the first signal and the second signal are not both at the first output node. None of the signals in Deering share a common output node. In contrast, each signal is received by a display 25 (page 11).

In reply, the Examiner points out that Taylor, which is the main reference, teaches that the first signal and the second signal are both at the first output node (Figure 1, 109, Col. 5, lines 1-3). Deering is merely used for its teaching of adjusting the second device until a value of the second signal substantially matches the determined value of the first signal. Since Deering teaches that the master emits the FIELD signal (first signal), thereby causing the slaves (second device) to reset the counters which produce video timing signals (second signal) so that the blanking occurs nearly simultaneously on different video display, this resetting of the counter is considered to be equivalent to adjusting the second device (slave) until a value of the second signal (video timing signal) substantially matches the determined value of the first signal (FIELD signal) so that the blanking of the second device's display (slave display) occurs nearly

simultaneously as the blanking of the first device's display (master display). Since Taylor teaches that the first signal and the second signal are both at the first output node, this concept of adjusting as taught by Deering can be implemented into the device of Taylor to modify it so that the second device is adjusted until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) in view of Normile (US005461679A).

10. With regard to Claim 1, Taylor discloses a video driver system comprising a first graphics device (103a, Figure 1; *two display control units 103, each display control unit 103 includes a display controller 104, each display controller 104 executes graphics functions such as line draws, polygon fills, color space conversion, display data interpolation and zooming, and video streaming,* Col. 4, lines 14-21, 52-57) having an input and a first video component output to provide a first video output component signal; a second graphics device (103b) having an input and a first video component output to provide a first video output component signal (*display controller 104 receives data, instructions and addresses across bus 102*, Col. 4, lines 50-52; *units 103 raster out data and refresh their corresponding screen regions*, Col. 5, line 65-Col. 6, line 1); a first video output port (109) coupled to the first video component output of the first graphics device and the first video component output of the second graphics device (*display driver 109 receives digital data from controller 104*, Col. 5, lines 1-3), as can be seen in Figure 1.

However, Taylor does not teach a second video output port coupled to the first video component output of the second graphics device. However, Normile discloses a first video device (401, Figure 4; *multiple video processing modules such as 401-404*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (412) to provide a first video output component signal (*modules 401-404 are coupled to a computer system bus 425 via control bus 412,* Col. 9, lines 15-17); a second video device (402) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (420) to provide a first video output component signal (*the structure of*

module 401 has equal application to each of the remaining compute modules such as 402-404, grant compute module 401 access to shared memory 405 over bus 420, Col. 10, lines 25-27, 55-57); a first video output port (425) coupled to the first video component output (412) of the first video device (401) (*modules 401-404 are coupled to a computer system bus 425 via control bus 412,* Col. 9, lines 15-17) and the first video component output (420) of the second video device (402) (*shared memory 405 is coupled to bus 425 and is further coupled to bus 420*, Col. 9, lines 48-50; Col. 10, lines 25-27, 55-57); and a second video output port (430) coupled to the first video component output (420) of the second video device (402) (*frame buffer 430 is directly coupled to the video bus 420,* Col. 10, lines 7-11, 25-27, 55-57). Since the first video component output 420 of the second graphics device 402 outputs video to display 440 (Col. 9, lines 20-24, 48-50; Col. 10, lines 7-19), there must inherently be a video output port connected to display 440 in order to output the video to display 440. Therefore, there is a second video output port coupled to the first video component output of the second video device.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Taylor to include a second video output port coupled to the first video component output of the second graphics device as suggested by Normile because Normile suggests the advantage of being able to output to two different displays at the same time (Col. 10, lines 7-19).

11. With regard to Claim 18, Taylor discloses a monitor (110, Figure 1) coupled to the first video output port (*DAC 109 receives digital data from controller 104 and outputs the analog data to drive display 110*, Col. 5, lines 1-3).

12. Claims 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) in view of Deering (US005963200A).

13. With regard to Claim 19, Taylor discloses a method of providing a video signal, the method comprising generating a first signal at a first device (103a, Figure 1; Col. 4, lines 14-21, 52-57), wherein the first signal is representative of a first video output component (Col. 5, line 65-Col. 6, line 1); providing the first signal to a first node (109); determining a value of the first signal at a first output node (*digital to analog converter pallete (display driver) 109 receives digital data from controller 104, and outputs analog data to drive display 110 in response*, Col. 5, lines 1-3); generating a second signal at a second device (103b), wherein the second signal is representative of a first video output component (Col. 4, lines 52-57); providing the second signal of the second device to the first output node (Col. 5, lines 1-3). Since the digital to analog converter receives digital data (first signal) from controller 104 (first output node) and outputs analog data to drive the display in response to the first signal from the first output node (Col. 5, lines 1-3), it must inherently determine a value of the first signal in order to output analog data, since it outputs analog data in response to the first signal. This means that the determined value of the first signal causes the digital to analog converter to output analog data.

However, Taylor does not teach adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node. However, Deering describes that the first graphics device (14, Figure 2) acts as a master to the second graphics device (14) and adjusting the second device until a value of the

second signal at the first output node substantially matches the determined value of the first signal at the first output node (*three systems, each of these systems includes a rendering controller 14,* Col. 3, lines 19-25; *system 1 is programmed to act as the master and system 2 is programmed to act as the slave, the master emits the FIELD signal and the slave systems receive it, system 1 becomes the source of the vertical interval timing reference, the slaves respond to the received FIELD signal by resetting the counters, the reset state is defined to be identical to the state which exists in the master RAMDAC at the time when it emits the transition in the FIELD signal*, Col. 5, lines 22-45). Since Deering teaches that the master emits the FIELD signal (first signal), thereby causing the slaves (second device) to reset the counters which produce video timing signals (second signal) so that the blanking occurs nearly simultaneously on different video display (Col. 5, lines 22-45), this resetting of the counter is considered to be equivalent to adjusting the second device (slave) until a value of the second signal (video timing signal) substantially matches the determined value of the first signal (FIELD signal) so that the blanking of the second device's display (slave display) occurs nearly simultaneously as the blanking of the first device's display (master display). Since Taylor teaches that the first signal and the second signal are both at the first output node (Figure 1, 109, Col. 5, lines 1-3), this concept of adjusting as taught by Deering can be implemented into the device of Taylor to modify it so that the second device is adjusted until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Taylor to include adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first

signal at the first output node as suggested by Deering because Deering suggests the advantage that the master provides a single timing reference (Col. 5, lines 22-45). A system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in the viewed images because the computers do not operate from a single timing reference (Col. 3, lines 12-18). Therefore, because the master provides a single timing reference, this method avoids exhibiting aberrations in the viewed images.

14. With regard to Claim 21, Taylor does not explicitly teach that the value of the first and second signals is a voltage value. However, Deering discloses that the value of the first and second signals is a voltage value (*RAMDAC 21 is coupled to the host bus through the rendering controller and translates data from the frame buffer to a signal which is converted by a DAC to analog signals representing voltage levels*, Col. 1, line 61-Col. 2, line 2).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Taylor so that the value of the first and second signals is a voltage value as suggested by Deering because Deering suggests that it is well-known in the art that the video output is controlled by voltage levels (Col. 1, line 61-Col. 2, line 2).

15. With regard to Claim 22, Taylor does not teach that the step of determining includes modifying and comparing the value of the first signal until the value of the first signal substantially matches a predetermined value. However, Deering discloses that the step of determining includes modifying and comparing the value of the first signal until the value of the

first signal substantially matches a predetermined value (Col. 5, lines 22-45). This would be obvious for the same reasons given in the rejection for Claim 19.

16. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1) in view of Lengyel (US006016150A), further in view of Taylor (US006118461A), further in view of Normile (US005461679A).

Walls discloses multiple graphics devices (202, 204, 206, 208, Figure 2), each having an input (203, 205, 207, 209) and operable to render video for an entire screen for one display device that displays a portion of the complete composite display, such that the combination of all of the display devices present the illusion of one large logical screen that displays the complete composite display (*a composite screen is constructed using numerous separate physical display devices, in other words, the different physical display devices comprising the composite screen must be controlled in concert so that they present the illusion of one large logical screen, this kind of functionality has become known as "single logical screen" functionality*, Col. 1, lines 28-31, 37-42; *X server 200 controls multiple display hardware devices 202, 204, 206 and 208 via buses 203, 205, 207 and 209, this capability is accomplished by the addition of a single-logical-screen layer, each of the physical display devices in the composite screen is driven by a separate graphics hardware system*, Col. 2, lines 19-26, 39-41). Since each graphics device is operable to render video for an entire screen for one display device (Col. 2, lines 39-41), each graphics device is considered to render an entire frame of video. Therefore, Walls discloses a video driver system comprising a first graphics device (202) having an input (203) and a first video component output to provide a first video output component signal; a second graphics device

(204) having an input (205) and a first video component output to provide a first video output component signal; wherein the first graphics device renders an entire frame of video, and wherein the second graphics device renders an entire frame of video.

However, Walls does not explicitly teach a first video output port coupled to the first video component output of the first graphics device and to the first video component output of the second graphics device. However, Lengyel discloses a first graphics device (56, Figure 2) operative to render a first portion (46) of a complete composite display (34); and a second graphics device (58) operative to render a second portion (48) of the complete composite display (*splits the scene into scene elements 46, 48, each of the independent scene elements have a corresponding renderer 56, 58, the diagram of the renderers 56, 58 represents that the scene elements are rendered independently*, Col. 7, lines 13-16, 66-67; Col. 8, lines 1-2). A compositor (60) is operatively coupled to receive the rendered video (50, 52; *the output of each rendering is a sprite 50, 52*, Col. 8, line 30) from any of the multiple graphics device and combines the input rendered video and outputs it to a first video output port (196, Figure 17) in order to ensure that the inputs to the compositing operation are synchronized (*the compositor receives the sprites and combines pixels in the sprites at corresponding screen coordinates into final pixel values*, Col. 8, lines 55-60; *compositing logic 192 sends its output to a demultiplexer 196, demultiplexer 196 transfers the pixel values from the compositing logic 192 to the selected buffer, by sending control signals 202 to the buffers, the memory control logic ensures that the inputs to the compositing operation are synchronized*, Col. 24, lines 7-13, 22-27). Therefore, a first video output port is coupled to receive the rendered video from the graphics devices. Therefore, by implementing this compositor taught by Lengyel into the device of Walls, the

device of Walls can be modified so that a first video output port is coupled to the first video component output of the first graphics device and to the first video component output of the second graphics device; and wherein the first graphics device renders video and provides the rendered video to the first video output port, and wherein the second graphics device renders video and provides the video to the first video output port in order to ensure that the inputs to the compositing operation are synchronized so that the output of the complete composite display is synchronized.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Walls to include a first video output port coupled to the first video component output of the first graphics device and to the first video component output of the second graphics device as suggested by Lengyel because Lengyel suggests the advantage of ensuring that the inputs to the compositing operation are synchronized so that the output of the complete composite display is synchronized (Col. 24, lines 7-13, 22-27).

However, Walls and Lengyel do not explicitly teach that the second graphics device renders an adjacent frame of video. However, Taylor describes that the frame from the frame buffer of display control unit 103a (Col. 5, line 65-Col. 6, line 1) is output first to the display (110) (Col. 6, lines 50-61), then the frame from the frame buffer of display control unit 103b (Col. 5, line 65-Col. 6, line 1) is output next to the display (Col. 7, lines 11-30). Since Claim 29 does not specify what the phrase "adjacent frames of video" means, the phrase "adjacent frames of video" is taken to mean that the second rendered frame is output immediately after the first rendered frame has been output, which is what Taylor teaches.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Walls and Lengyel so that the second graphics device renders an adjacent frame of video as suggested by Taylor because Taylor suggests that since the first and second rendered frames are provided to a common port (109; Col. 5, lines 1-3 in Taylor), as is also taught in Lengyel as discussed above, this means that only one rendered frame can be output to the common port at a time, and therefore the first rendered frame is output first, then the second rendered frame is output immediately after the first rendered frame has been output (Col. 2, line 58-Col. 3, line 15; Col. 6, lines 50-61; Col. 7, lines 11-30), and therefore the first and second rendered frames are adjacent frames of video.

However, Walls, Lengyel, and Taylor do not teach a second video output port coupled to the first video component output of the second graphics device. However, Normile describes a video driver system comprising a first video device (401, Figure 4, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (412) to provide a first video output component signal (*modules 401-404 are coupled to a computer system bus 425 via control bus 412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller 426*, Col. 9, lines 15-24); a second video device (402, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (420) to provide a first video output component signal; a first video output port (425) coupled to the first video component output of the first video device and the first video component output of the second video device (*modules 401-404 are coupled to a*

computer system bus 425 via control bus 412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller 426, Col. 9, lines 15-24, 48-50; Col. 10, lines 7-19); and a second video output port (440) coupled to the first video component output of the second video device (Col. 10, lines 7-19). This would be obvious for the same reasons given in the rejection for Claim 1.

17. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1) in view of Lengyel (US006016150A).

Walls discloses multiple graphics devices (202, 204, 206, 208, Figure 2), each operable to render video for an entire screen for one display device that displays a portion of the complete composite display, such that the combination of all of the display devices present the illusion of one large logical screen that displays the complete composite display (Col. 1, lines 28-31, 37-42; Col. 2, lines 19-26, 39-41). Since each graphics device is operable to render video for an entire screen for one display device (Col. 2, lines 39-41), each graphics device is considered to render an entire frame of video. Therefore, Walls discloses an apparatus for providing video signals comprising a first graphics device (202) operative to render an entire first frame of video; and a second graphics device (204) operative to render an entire second frame of video.

However, Walls does not explicitly teach a common port, operatively coupled to receive the first and second frames of rendered video from either of the first and second graphics devices. However, Lengyel discloses a first graphics device (56, Figure 2) operative to render a first portion (46) of a complete composite display (34); and a second graphics device (58) operative to render a second portion (48) of the complete composite display (Col. 7, lines 13-16,

66-67; Col. 8, lines 1-2). A compositor (60) is operatively coupled to receive the rendered video (50, 52; Col. 8; line 30) from any of the multiple graphics device and combines the input rendered video and outputs it to a common port (196, Figure 17) in order to ensure that the inputs to the compositing operation are synchronized (Col. 8, lines 55-60; Col. 24, lines 7-13, 22-27). Therefore, a common port is operatively coupled to receive the rendered video from any of the graphics devices. Therefore, by implementing this compositor taught by Lengyel into the device of Walls, the device of Walls can be modified so that a common port is operatively coupled to receive the first and second frames of rendered video from either of the first and second graphics devices in order to ensure that the inputs to the compositing operation are synchronized so that the output of the complete composite display is synchronized. This would be obvious for the same reasons given in the rejection for Claim 29.

18. Claims 31, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1) and Lengyel (US006016150A) in view of Taylor (US006118461A).

19. With regard to Claim 31, Walls and Lengyel are relied upon for the teachings as discussed above relative to Claim 30.

However, Walls and Lengyel do not explicitly teach a first frame buffer operatively coupled to the first graphics device and a second frame buffer operatively coupled to the second graphics device. However, Taylor discloses multiple graphics devices (103, Figure 1), each operable to render video for a portion of the complete composite display (Col. 4, lines 14-21, 52-57; Col. 5, line 65-Col. 6, lines 1). A first frame buffer is operatively coupled to the first

graphics device and a second frame buffer is operatively coupled to the second graphics device (*two display control units 103,* Col. 4, lines 14-18, *each display control unit 103 includes a frame buffer 105*, Col. 4, lines 19-21).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Walls and Lengyel to include a first frame buffer operatively coupled to the first graphics device and a second frame buffer operatively coupled to the second graphics device as suggested by Taylor because Taylor suggests that while images are in the process of being drawn and are not yet ready to be displayed, the frame buffer can store the graphics data defining the color/gray-shade of each pixel of an entire display frame, so that when the image is ready to be displayed, the pixel data can immediately be retrieved out of the frame buffer as the corresponding display pixels on the display screen are being generated (Col. 1, lines 40-46).

20. With regard to Claim 38, Walls and Lengyel do not explicitly teach that the first graphics device and second graphics devices are video graphics adapters. However, Taylor describes that the first graphics device and second graphics devices (*two display control units 103*, Col. 4, lines 14-18) are video graphics adapters (*each display control unit 103 includes a display controller 104, Col. 4, lines 19-20, display controller 104 may be VGA controller*, Col. 4, line 49).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Walls and Lengyel so that the first graphics device and second graphics devices are video graphics adapters as suggested by Taylor because Taylor suggests that video graphics adapters are a well-known type of graphics device (Col. 1, lines 32-39; Col. 4,

lines 46-50). A majority of manufacturers have conformed to the VGA graphical standard, making it the lowest common denominator that all PC graphics hardware supports. Therefore, the majority of PC graphics hardware would have video graphics adapters, and therefore video graphics adapters are well-known in the art and widely used.

21. With regard to Claim 39, Walls and Lengyel do not explicitly teach that the first and second rendered frames are adjacent frames of video. However, Taylor describes that the frame from the frame buffer of display control unit 103a (Col. 5, line 65-Col. 6, line 1) is output first to the display (110) (Col. 6, lines 50-61), then the frame from the frame buffer of display control unit 103b (Col. 5, line 65-Col. 6, line 1) is output next to the display (Col. 7, lines 11-30). Therefore, Taylor describes that the first and second rendered frames are adjacent frames of video. Since Claim 39 does not specify what the phrase "adjacent frames of video" means, the phrase "adjacent frames of video" is taken to mean that the second rendered frame is output immediately after the first rendered frame has been output, which is what Taylor teaches. This would be obvious for the same reasons given in the rejection for Claim 29.

22. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1), Lengyel (US006016150A), and Taylor (US006118461A).
in view of Deering (US005963200A).

Walls, Lengyel, and Taylor are relied upon for the teachings as discussed above relative to Claim 31.

However, Walls does not explicitly teach at least one digital to analog converter operatively coupled to output video. However, Lengyel discloses at least one digital to analog converter (244, Figure 19) operatively coupled to output video (*DAC controls the routing of pixel data to the display monitor 248*, Col. 30, lines 39-48).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Walls to include at least one digital to analog converter operatively coupled to output video as suggested by Lengyel because Lengyel suggests that digital to analog converters are well-known in the art (Col. 30, lines 39-48). Video signals from a digital source, such as a computer, must be converted to analog form if they are to be displayed on an analog monitor, and therefore a digital to analog converter is needed. Digital to analog converters are well-known in the art and widely used.

However, Walls, Lengyel, and Taylor do not teach having voltage adjusted in order to correlate video out voltages being provided by at least one of the graphics devices. However, Deering describes that the first graphics device (14, Figure 2) acts as a master to the second graphics device (14) and adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node in order to correlate video out being provided by at least one of the graphics devices (Col. 3, lines 19-25; Col. 5, lines 22-45). Deering discloses that the value of the first and second signals is a voltage value (Col. 1, line 61-Col. 2, line 2). This would be obvious for the same reasons given in the rejection for Claims 19 and 21.

23. Claims 33, 34, 36, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1) and Lengyel (US006016150A in view of Deering (US005963200A).

24. With regard to Claim 33, Walls and Lengyel are relied upon for the teachings as discussed above relative to Claim 30.

However, Walls and Lengyel do not teach a circuitry operative to provide digital to analog conversion voltage equalization associated with the first and second graphics devices. However, Deering describes an apparatus for providing video signals comprising a first graphics device (14, Figure 2) operative to render a first frame of video and a second graphics device (14) operative to render a second frame of video. Deering describes a circuitry operative to provide digital to analog conversion frequency equalization (*synchronizes events produced in the video timing generator circuits of the three RAMDACs*, Col. 5, lines 12-16). The frequencies produced by the RAMDACs will vary within a range of values which depends on voltage (Col. 4, lines 57-63). Adjusting the frequency means adjusting the voltage. This is well-known in the art, and can be found in many publications, such as Wunner (US005095280A) (*the VCO to adjust up or down to the new selected frequency*, Col. 8, lines 1-14). Therefore, Deering describes a circuitry operative to provide digital to analog conversion voltage equalization.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Walls and Lengyel to include a circuitry operative to provide digital to analog conversion voltage equalization associated with the first and second graphics devices as suggested by Deering because Deering suggests that a system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers

may exhibit aberrations in the viewed images because the computers do not operate from a single timing reference (Col. 3, lines 12-18). Therefore, it is advantageous to include a circuitry operative to provide digital to analog conversion frequency or voltage equalization because it avoids exhibiting aberrations in the viewed images.

25. With regard to Claim 34, Walls does not explicitly teach outputting video from the second graphics device to the common port. However, Lengyel discloses outputting video from the second graphics device to the common port, as discussed in the rejection for Claim 30.

However, Walls and Lengyel do not teach that the first graphics device includes a controller operative to select video from the second graphics device to be output. However, Deering describes a master graphics device and a slave graphics device (Col. 5, lines 22-25). The master graphics device emits the FIELD signal and the slave graphics device receives it (Col. 5, lines 25-27). The slave graphics device responds to the received FIELD signal by resetting the counters which produce the video timing signals (Col. 5, lines 30-33). Therefore, Deering describes that the first graphics device includes a controller operative to select video from the second graphics device to be output.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Walls and Lengyel so that that the first graphics device includes a controller operative to select video from the second graphics device to be output as suggested by Deering because Deering suggests that this is how a master-slave system works (Col. 5, lines 22-33). Deering suggests that a master-slave system is advantageous because the master provides a single timing reference (Col. 5, lines 22-45). A system utilizing two or more

video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in the viewed images because the computers do not operate from a single timing reference (Col. 3, lines 12-18). Therefore, because the master provides a single timing reference, this method avoids exhibiting aberrations in the viewed images.

26. With regard to Claim 36, Walls and Lengyel do not teach that the first graphics devices acts as a master to the second graphics device and provides synchronization control for the second graphics device. However, Deering describes that the first graphics device (14, Figure 2) acts as a master to the second graphics device (14) and provides synchronization control for the second graphics device (Col. 3, lines 19-25; *the slaves respond to the received FIELD signal by resetting the counters which produces the video timing synch signals, the reset state is defined to be identical to the state which exists in the master RAMDAC at the time when it emits the transition in the FIELD signal, thus achieving the required synchronization*, Col. 5, lines 22-45).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Walls and Lengyel so that the first graphics devices acts as a master to the second graphics device and provides synchronization control for the second graphics device as suggested by Deering because Deering suggests the advantage that the master provides a single timing reference (Col. 5, lines 22-45). A system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in the viewed images because the computers do not operate from a single timing reference (Col. 3, lines 12-18). Therefore, because the master provides a single timing reference, this method avoids exhibiting aberrations in the viewed images.

27. With regard to Claim 37, Walls and Lengyel do not teach that the first graphics device includes a reference signal generator for the second graphics controller. However, Deering describes that the first graphics devices includes a reference signal generator for the second graphics controller (*system 1 becomes the source of the vertical interval timing reference*, Col. 5, lines 22-45), as discussed in the rejection for Claim 36.

28. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1) and Lengyel (US006016150A) in view of Eichenberger (see Prior Art of Record below).

Walls and Lengyel are relied upon for the teachings as discussed above relative to Claim 30.

However, Walls and Lengyel do not teach a load operatively couplable to either one of first and second graphics devices when at least one of the first and second graphics devices is not driving the common port. However, Eichenberger describes the use of a dummy switch with a load coupled to it for charge cancellation of the active switch (pp. 257, 260). In other words, the switch that is not active or is not driving the common port acts as the dummy switch and has a load coupled to it.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Walls and Lengyel to include a load operatively couplable to either one of first and second graphics devices when at least one of the first and second graphics devices is not driving the common port as suggested by Eichenberger because Eichenberger

suggests the advantage of reducing charge injection by charge cancellation (page 257). The advantages of using dummy switches is well-known in the art and can be found in many publications.

Allowable Subject Matter

29. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

30. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken singly or in combination do not teach or suggest a method comprising the step of removing the first signal from the first node prior to the step or providing the second signal as recited in Claim 20. This claim is similar to Claim 19 of U.S. patent 6,424,320, to which this application is a continuation of.

Prior Art of Record

C. Eichenberger, W. Guggenbuhl, "On Charge Injection in Analog MOS Switches and Dummy Switch Compensation Techniques," *IEEE Transactions on Circuits and Systems*, vol. 37, pp. 256-264, 1990.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kehlet (US005956046A) describes a video system comprising a first frame buffer (202A, Figure 3) having an input (Col. 5, lines 49-51) and a first video component output (222A) to provide a first video output component signal (Col. 5, lines 51-53); a second frame buffer (202B) having an input (Col. 5, lines 49-51) and a first video component output (222B) to provide a first video output component signal (Col. 5, lines 51-53); a first video output port (220) coupled to the first video component output of the first frame buffer and to the first video component output of the second frame buffer (Col. 5, lines 51-53); wherein the first frame buffer has a rendered frame of video and provides the rendered frame to the first video output port, and wherein the second frame buffer has a rendered adjacent frame of video and provides the adjacent frame to the first video output port (Col. 6, lines 13-22).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

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